Polytech network form for PhD Research Grants from the China Scholarship Council

This document describes the PhD subject and supervisor proposed by the French Polytech network of 14 university engineering schools. Please contact the PhD supervisor by email or Skype for further information regarding your application.

Supervisor information	
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Country	France

PhD information	
Title	High efficiency CMOS charge pumps for IoT and other low-power applications
Main topics regards to CSC list (3 topics at maximum)	I-14 IC Design ; I-3 Micro(nano) electronic components

Required skills in science and engineering	Analog Circuit Design – Transistor-level circuit design – IC Design

Subject description (two pages maximum)

Title of the research proposal: High efficiency CMOS charge pumps for IoT and other low-power applications

Keywords: CMOS analog circuits, High-efficiency, low-power consumption, Charge pumps

Abstract: the microelectronics roadmap towards higher integration of components, the so-called moore's law, leads to ever smaller transistors with lower power supply voltages and smaller power consumption per transistor. However, a lot of applications require higher voltage than the one fixed by the power supply and level shifters or pump charges are often required to multiply these voltages by one order of magnitude or even more. Among those applications one can cite the Internet of Things (IoT) and more particularly embedded sensors and/or actuators that often require voltages in the range between 10 up to 100V.

Starting from the Dickson's charge pump in the late 70s (1), numerous charge pump architectures have been proposed to improve the overall efficiency (2, 3, 4) but all this research focuss on a quasi-constant power delivery at the output of the charge pump while in the targeted applications power delivery is only required in a short amount of time when, for example, electrostatic actuation is required. The purpose of this research is to decline the principle of charge pumps for resistive "constant" loads to propose a smart charge pump able to deliver some bursts of output power with a very good efficiency. This objective may be reached by adding a control circuitry to the charge pump able to stop pumping when output current is small or close to zero.

The research program extends on the total duration of the PhD curriculum as follows:

1) Review of the literature and identification of the best candidates among the existing charge pumps,
2) Study of pumping-control architectures that may improve power efficiency of the identified charge pumps for bursted-power delivery,
3) Validation at the structural level of the proposed smart-architecture: electrical simulation and transistor-level simulations,
4) Layout of a silicon prototype – fabrication using an industrial fabrication technology,
5) Characterization of the experimental prototype
6) Dissemination of results and thesis preparation.

References

(1) J.F. Dickson, *"On-chip high voltagegeneration in NMOS integrated circuit using an improved voltage multiplier techniques",* IEEE J.Solid-state Circuits , vol.11, pp.374- 378, June, 1976

(2) Jongshin Shin et al., *"A New Charge Pump without Degradation in Threshold Voltage Due to Body Effect",*, IEEE J. Solid-state Circuits, Vol. 35, No. 8, pp. 1227- 1230, August, 2000

(3) M. Zhang and N. Llaser, *"Low-Voltage Charge Pump"*, Electronics Letters, Vol.42, February, 2006

(4) J. Heitz, N. Dumas, V. Frick, C. Lallement and L. H́ebrard, *"Modeling and Optimization of a Ker Charge Pump Loaded by a Resistive Circuit"*, IEEE Conference Mixed Design of Integrated Circuits and Systems, War- saw, 24-26 May 2012