Polytech network form for PhD Research Grants from the China Scholarship Council

This document describes the PhD subject and supervisor proposed by the French Polytech network of 14 university engineering schools. Please contact the PhD supervisor by email or Skype for further information regarding your application.

Supervisor information	
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PhD information	
Title	Design and realization of a BLE Transceiver in FDSOI Technology
Main topics regards to CSC list (3 topics at maximum)	**Telecommunication and information Technology**

	Nanoelectronics IC Design
Required skills in science and engineering	Electronics and microelectronics EDA Tools (Spice, Cadence) Analog and RF circuit design

Subject description (two pages maximum)

Subject Thesis :

- As a first step

The candidate will have to familiarize himself with the FDSOI technology and Cadence software. It will thus resume the work carried out by Zhaopeng Wei, on the simulation under Cadence (transients, Monte Carlo, phase noise, ...) of the basic blocks of a PLL. In the case of ring oscillators (aka RO) or voltage-controlled ring oscillators (VCRO) based on inverter chains, to decrease the jitter, it is important that the transistors have the same characteristics. Moreover, if the rise and fall times (tpLH and tpHL) are the same, the performances of the oscillator will be better. By using differential logic and the back-gate of FDSOI transistors, we can meet this first target (the NMOS transistor, faster, will accelerate the conduction of the transistor PMOS, slower, and reciprocally) , and on the other hand realize a ring oscillator with an even number of inverters (which is impossible with standard logic).

- Optimization of the design of a VCRO and PLL

By reusing again the work of Zhaopeng Wei, the first work will be to optimize the VCRO, this time for a central frequency of 2, 45GHz (Standard BLE). The VCRO is known to be very effective in terms of area and consumption but exhibits a phase noise not compatible to many applications. The idea behind this study is, first, to implement the technique of self-biasing of the back-gate of the FDSOI transistor to decrease the jitter. We have also already designed the basic blocks, in FDSOI, which form a PLL using the complementary logic. We use the control of the threshold voltage of the transistors that this technology offers us through the back-gate as well as a new form of logic based on this principle. We have designed the main base blocks that make up the PLL starting from scratch and imposing as the limit that of FDSOI technology 28 nm.

- Mixer Design

It is expected in the first year of thesis to also design a mixer. A study of the art will allow to identify the best circuits as well as their associated performances. The peculiarities of the FDSOI technology should make it possible to achieve a new topology: a single transistor should be able to achieve this function by using the two gates as input of the multiplier (the gate for the signal, output of the LNA, and the back-gate for the local oscillator, output of the PLL). Simulations under Cadence will optimize this circuit and the sizing of the components.

- Physical realization

The second year will be devoted, in a first step, to the drawing of the masks (layout) of the complete PLL circuit and mixer. The first test circuits will be defined by the two partners, they will have to include at least a Ring oscillator with at least four quadrature output, as well as a VCRO, mixer and PLL. The connection between the two circuits can be done in an external way. The laboratory's PhD student will benefit from the expertise of some members of the LETI in terms of layout skills on FDSOI Technology 28 nm. This will lead to the realization of all or part of this layout at LETI. Feedback, measurements, will validate and finalize the optimization of the design of a complete PLL and mixer. The LETI will bring its know-how to carry out the measurements on the circuits in return of foundry.

- Design of the LNA

In parallel with the realization of the layout and test of the first circuit, the Ph.D. student will begin in the second year to study various topologies of LNA to retain an efficient and transposable topology to the FDSOI technology, if none exists in this Technology. The first simulations will continue in the last year, which will be devoted to the realization and testing of this final circuit, as well as to the writing of thesis dissertation.

Thesis Context :

The variability of the manufacturing processes of integrated circuits (analog, digital or mixed) raises issues in their design and implementation in advanced technologies (32 nm and beyond). This variability introduces mismatches of the transistors, so on the same "wafer", even on the same chip, the supposed identical transistors do not show the same characteristics. This difference in characteristics can introduce malfunctions of the final circuit, that may no longer match, for some applications, the required specifications. In the specific case of analog electronics, some cells require transistors to be perfectly identical (paired): current mirrors, differential pairs, ... Calibration techniques have become necessary for most applications. The implementation of this calibration increases the area and consumption of the final circuit, therefore its cost.

As part of the 'Fully Depleted Silicon On Insulator' (aka FDSOI) technology, we propose to use the back-gate of MOS transistors to perform this calibration automatically (by self-biasing) on symmetrical (or differential) cells. This process is also used to reduce mismatches between components (transistors) and to "mirror" certain cells (e.g. PMOS and NMOS of a differential inverter) without increasing the surface and consumption of the circuit.

CEA-LETI Grenoble and the Laboratory Polytech'Lab have collaborated for several years on the design of circuits in Silicon On Insulator technology (PDSOI, then FDSOI, see Common Publications). Zhaopeng Wei, Chinese PhD student, is currently working on the design and realization of a PLL based on this concept of self-biased of the FDSOI transistor back-gate. This work has already given rise to 12 publications (an international journal, 9 international conferences including 3 as a guest, 1 national conference and 1 patent filing). He is currently writing his dissertation and should support in December 2018. The aim of this new project is to continue this collaborative work by integrating the receiving part of an RF transceiver for an BLE (BlueTooth Low Energy) application for example, designing and realizing the LNA, as well as the mixer, to which will be added the PLL previously performed.

Scientific officer Polytech'Lab : Gilles Jacquemod
Scientific Officer CEA-LETI: Emeric de Foucauld

Presentation of the Laboratory : The Polytech'Lab Laboratory is the research unit of the Nice-Sophia Polytech School, at the University of Nice Sophia Antipolis, a member of the "University of the Côte d'Azur". Created in January 2017 with the merger of two I-City Laboratories (URE UNS 006) and EpOC (URE UNS 007), this laboratory also hosts a team of the Smart Buildings Department of the school. In February 2018, it was labelled by the Ministry of Higher Education EA 7498.
The main research activities of this laboratory, oriented towards the socio-economic world and the industrial transfer, are focused on the management of energy, water and risk around the concept of smart city, using information and communication technologies. Polytech'Lab's strategy is based on three pillars: (i) an ambitious and disruptive scientific vision; (ii) a privileged relationship with the socio-economic world whether companies or local and regional authorities; (iii) a very strong synergy between education, research and innovation.
The research domains range from the connected objects (sensors and sensor networks) to the smart city passing through the smart building with the development of several fields. In the field of microelectronics, these axes are:

- Reliability and characterization of non-volatile and CEM memories IC
- New technologies for very low consumption
- Front-end RF, sensors, very high-speed links, small cells 5G, ...

Presentation of CEA LETI institute : Leti, a technology research institute at CEA Tech, pioneers micro and nanotechnologies, tailoring differentiating applicative solutions that ensure competitiveness in a wide range of markets. The institute tackles critical challenges such as healthcare, energy, transport and ICTs.
Its multidisciplinary teams deliver solid expertise for applications ranging from sensors to data processing and computing solutions, leveraging world-class pre-industrialization facilities.
Leti builds long-term relationships with its industrial partners - global companies, SMEs and startups – and actively supports the launch of technology startups.
Leti's main divisions: Architecture and IC design, embedded software, Silicon components, Silicon technologies, Optics and Photonics, Technologies for Biology and Health, Systems and solutions integration
CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in research, development and innovation in defense & security, nuclear energy, technological research for industry and fundamental physical and life sciences. In 2015, Thomson Reuters identified CEA as the most innovative research organization in the world.

Joint Publication between Polytech'Lab and CEA-LETI in the field of:

A- Patents:

1. G. Jacquemod, E. de Foucauld, Y. Leduc, A. Fonseca & P. Lorenzini "method and device for autocalibration of Multigrid circuits", French patent UNS and CEA-LETI, 10 April 2015, FRA 1553096, extended Europe, 8 April 2016, 16164459.6 -1810, extension USA, 13 October 2016, US20160301365
2. P. Audebert, E. de Foucauld, Y. Leduc, G. Jacquemod, Z. Wei & P. Lorenzini, "Basic electronic Circuit for amplification or copying of analogue signals", French patent CEA-LETI et UNS, 6 April 2017, WO2017055709 A1, PCT/FR2016/052394

B- International journals:

3. L. Geynet, E. de Foucauld, P. Vincent & G. Jacquemod, «Fully-Integrated Dual-Band VCOs with Power Controlled by Body Voltage in 130nm CMOS/SOI for Multi-Standard Applications», Analog Integrated Circuits and Signal Processing, vol. 53, n° 1, 2007, p. 43-51
4. G. Jacquemod, L. Geynet, B. Nicolle, E. de Foucauld, W. Tatinian & P. Vincent, «Design and Modelling of a Multistandard Fractional PLL in CMOS/SOI Technology», Microelectronics Journal, vol. 39, n° 9, 2008, p. 1130-1139
5. A. Fonseca, E. de Foucauld, P. Lorenzini & G. Jacquemod, «Low power 28nm FDSOI 2.45 GHz PLL», Journal of Low Power Electronics, vol. 10, n° 1, 2014, p. 149-162
6. G. Jacquemod, A. Fonseca, E. de Foucauld, Y. Leduc & P. Lorenzini, "2.45 GHz 0.8 mW voltage-controlled ring oscillator (VCRO) in 28 nm Fully Depleted Silicon On Insulator (FDSOI) Technology», Frontiers of Materials Science, vol. 9, Issue 2, 2015, p. 156-162
7. Z. Wei, G. Jacquemod, P. Lorenzini, F. Hameau, E. de Foucauld & Y. Leduc, «Study and reduction of variability in 28nm Fully Depleted Silicon on Insulator technology», Journal of Low Power Electronics, vol. 12, n° 1, 2016, p. 64-73

C- Guest Lectures:

8. A. Fonseca, E. de Foucauld, P. Lorenzini & G. Jacquemod, «CMOS technology beyond 22 nm», ICSS, Las Vegas, 2013, p. 152-153
9. G. Jacquemod, A. Fonseca, Y. Leduc, E. de Foucauld & P. Lorenzini, «Analog Design in FDSOI 28 nm technology and beyond», BIT's 3rd Annual World Congress of Emerging InfoTech, Dalian, 2014, p. 112
10. A. Fonseca, G. Jacquemod, Y. Leduc, E. de Foucauld & P. Lorenzini,, «VCO Design in SOI technologies», NEWCAS, Special Session «Frequency synthesis – New designs, new technologies», Trois Rivières, 2014, p. 420-423
11. G. Jacquemod, A. Fonseca, E. de Foucauld, Y. Leduc & P. Lorenzini, "2.45 GHz 0.8 MW VCRO in 28nm FDSOI Technology", ICSS, Hong Kong, 2014, pp. 74-75
12. G. Jacquemod, Y. Leduc P. Lorenzini, E. de Foucauld, & A. Fonseca, «Self-calibration of analog and mixed cells using back-gate auto-biasing transistor in 28nm FDSOI Technology and beyond», Nanotechnology and Materials Science, Dubai, 2015, p. 97
13. Y. Leduc, Z. Wei, J. Modad, M.A. Garcia Perez, E. de Foucauld, P. Lorenzini & G. Jacquemod, «Digital complementary logic in 28 nm FDSOI to address the next nanoelectronic challenges», BIT's, 5th Annual World Congress of Nano Science & Technology, Xi'an, 2015, p. 172

14. G. Jacquemod, E. de Foucauld, Y. Leduc, F. Hameau, Z. Wei, J. Modad & P. Lorenzini, «VCRO design in 28 nm FDSOI technology using fully complementary inverters », ICSS, Phuket, Thailland, 2015, p. 62-64
15. Y. Leduc, G. Jacquemod, Z. Wei, J. Modad, P. Lorenzini, & E. de Foucauld, "complementary logic, an opportunity offered by the FDSOI for integrating mixed circuits into the most advanced technologies", FETCH, Villard-de-Lans, France, 2016

D- International conferences:

16. L. Geynet, E. de Foucauld, D. Cartalade, P. Vincent & G. Jacquemod, «Design of a fully-integrated multi-band VCO for wireless applications in 130nm CMOS/SOI», SAME, Sophia Antipolis, 2004, p. 58-61
17. L. Geynet, E. de Foucauld, P. Vincent & G. Jacquemod, «A fully-Integrated Dual-Band VCO with Power Controlled by Body Voltage in 130 nm CMOS/SOI», IEEE-NEWCAS, Montreal, 2005, p.195-198
18. L. Geynet, E. de Foucauld, D. Cartalade & G. Jacquemod, «An Integrated Balun for Dual-Band LC tank VCO in 130nm CMOS/SOI», IEEE SOI Conference, Honolulu, 2005
19. B. Nicolle, L. Geynet, E. de Foucauld, P. Vincent, W. Tatinian & G. Jacquemod, «High Level Modelling of ΣΔ Fractional PLL for Noise Estimation», SAME, Sophia Antipolis, 2005
20. B. Nicolle, L. Geynet, E. de Foucauld, W. Tatinian & G. Jacquemod, «VHDL-AMS Modeling of multi-standard Phase Locked Loop», ICECS, Gammarth, 2005, p.33-36
21. L. Geynet, E. de Foucauld, P. Vincent & G. Jacquemod, «Fully-Integrated Multistandard VCOs with switched LC tank and Power Controlled by Body Voltage in 130nm CMOS/SOI», RFIC, San Francisco, 2006, p.109-112
22. A. Fonseca, E. de Foucauld, P. Lorenzini & G. Jacquemod, «Process variation compensation for PLL on FDSOI 28nm», VARI/PATMOS, Karlsruhe, 2013
23. A. Fonseca, E. de Foucauld, P. Lorenzini & G. Jacquemod, «Fractional phase divider PLL phase noise and spurious modeling», VARI/PATMOS, Palma de Mallorca, 2014
24. G. Jacquemod, Z. Wei, J. Modad, E. de Foucauld, F. Hameau, Y. Leduc & P. Lorenzini, «Study and reduction of variability in 28 nm FDSOI technology», VARI/PATMOS, Salvador de Bahia, Brazil, 2015, p. 19-22
25. Z. Wei, Y. Leduc, G. Jacquemod & E. de Foucauld, «UTBB-FDSOI Complementary Logic for High Quality Analog Signal Processing», ICECS, Monaco, 2016
26. Z. Wei, Y. Leduc, E. de Foucauld & G. Jacquemod, «Novel Building Blocks for PLL Using Complementary Logic in 28nm UTBB-FDSOI Technology», NewCAS, Strasbourg, France, 2017, p. 121-124
27. G. Jacquemod, Z. Wei, Y. Leduc & E. de Foucauld, «Back-gate cross-coupled cells for high performance clock in 28nm FDSOI technology», Annual World Congress of Nano Science & Technology, Fukuoka, Japan, 2017
28. Z. Wei, G. Jacquemod, J. proves, E. de Foucauld & Y. Leduc, Low Power IoT Design using FDSOI Technology", SENSO, Gardanne, 2017